AMENDMENT

In the drawings:

The Applicants' attorney has changed multiple occurrences of "Hardware Pipeline" to "Hardwired Pipeline" in FIG. 3, and enclose amended FIG. 3 labeled Replacement Sheet. The changes add no new matter to the figures.

REMARKS

Claims 1 – 27 are pending. Claims 1, 4, 11, and 15-22 are currently amended, although the amendments to claims 16-22 do not narrow these claims, and claims 23-27 are new. As discussed below, the claims are in condition for allowance. **But if after considering this response the Examiner does not agree that all of the claims are allowable, he is respectfully requested to schedule and conduct a telephone interview with the Applicants' attorney before issuing a subsequent Office Action.**

Objection to the Title of the Patent Application

The Applicants' attorney requests that the title be changed to "Pipeline Accelerator Including Pipeline Circuits In Communication Via A Bus, And Related System And Method," and that the Examiner approve this new title.

Rejection of the Specification

The Applicants' attorney has corrected errors and added information missing from the text of the specification, and encloses a marked-up version of the amended text.

The Applicants' attorney has changed multiple occurrences of "Hardware Pipeline" to "Hardwired Pipeline" in FIG. 3, and encloses an amended version of FIG. 3.

But the changes to the specification and to FIG. 3 add no new matter to the patent application.

Rejection of Claims 1-3, 5-7, 9-13, and 15-22 Under 35 U.S.C. § 102(b) In View of U.S. Patent 6,282,627 to Wong

As discussed below, the Applicants' attorney respectfully disagrees with this rejection.

Claim 1

Claim 1 as amended recites a plurality of pipeline units each comprising a respective hardwired-pipeline circuit that is operable simultaneously with and asynchronously relative to at least one of the other hardwired-pipeline circuits.

For example, referring to FIGS. 4 and 6 of the patent application, a plurality of pipeline units 78 each comprise a respective hardwired-pipeline 74 that is operable simultaneously with and asynchronously relative to at least one of the other hardwired-pipelines 74. More specifically, a first hardwired-pipeline 74 on a pipeline unit 78_1 is operable to process data according to a first clock signal at the same time that a second hardwired-pipeline 74 on a pipeline unit 78_n processes data according to a second clock signal that is unsynchronized with the first clock signal.

In contrast, Wong does not disclose a hardwired-pipeline circuit that is operable simultaneously with and asynchronously relative to another hardwired-pipeline circuit. Referring, *e.g.,* to FIG. 6, although Wong's Datapath Program Units (DPUs) 621a and 621b may operate simultaneously, these DPUs are clocked by a common signal distributed via the Clock Distribution bus 609, and thus operate synchronously, not asynchronously like the two hardwired-pipelines recited in claim 1.

Claims 2-3, 5-7, and 9-10

These claims are patentable by virtue of their dependencies from claim 1.

Claim 11

Claim 11 as amended recites a processor, hardwired-pipeline circuits, and a pipeline bus coupled to the processor and to the hardwired-pipeline circuits (via a communication bus and a pipeline-bus interface) and operable to carry data and hardwired-pipeline-configuration information.

For example, referring, to FIG. 3 of the patent application, a pipeline bus 50 is operable to carry data between a host processor 42 and the hardwired pipelines 74 on a pipeline accelerator 44, and is operable to carry configuration

data from the host processor to the pipeline accelerator, which uses the data to configure the hardwired pipelines.

In contrast, Wong does not disclose a bus coupled to a processor and hardwired-pipeline circuits and operable to carry both data and hardwired-pipeline-configuration information. Referring, *e.g.,* to FIG. 16, col. 7, lines 30-35, col. 8, lines 15-16, and col. 8, lines 57-65, the bus between the ALU (processor) and the Adaptive Compute Module (ACM) carries data, but no configuration data (configuration information). Instead, as best understood by the Applicants' attorney, one or more other busses carry configuration data from the Local Store Memory (LSM) to the ACM to configure the DPUs (FIG. 6, hardwired-pipeline circuits) on the ACM.

Claims 12-13

These claims are patentable by virtue of their dependencies from claim 11.

Claim 15

Claim 15 as amended recites processing second data with a second pipeline unit asynchronously with respect to a first pipeline unit and while the first pipeline unit is processing first data.

Consequently, claim 15 is patentable for reasons similar to those recited above in support of the patentability of claim 1.

Claims 16-22

These claims are patentable by virtue of their dependencies from claim 15.

Rejection of Claims 4, 8, and 14 Under 35 U.S.C. § 103(a) In View of Wong

Claim 4

Claim 4, which the Applicants' attorney amended to be in independent form, recites hardwired-pipeline circuits disposed on respective field-programmable gate arrays.

For example, referring to FIG. 3, two or more of the hardwired pipelines 74 may be disposed on respective field-programmable gate arrays (FPGAs).
In contrast, not only does Wong teach away from disposing hardwired-pipeline circuits on multiple FPGAs, Wong does not suggest this even if the teaching away is disregarded.

Regarding the teaching away, col. 1, lines 52-54, col. 2, lines 48-50, and col. 5, lines 40-43 include but a few of the disparaging remarks Wong makes about FPGA technology (*i.e.*, the configurable architecture within an FPGA). Furthermore, nowhere does Wong temper these remarks by, for example, stating or suggesting that FPGA technology may be suitable for use in his architecture. Furthermore, disregarding Wong's teaching away for the moment, even if it were obvious to replace Wong's DPUs (FIG. 6) with FPGA technology, it would not be obvious to replace the DPUs with respective FPGAs (*i.e.*, FPGA chips). The Examiner seems to be confusing FPGA technology with FPGAs chips. Wong discloses a single-chip, not a multi-chip, architecture. Therefore, although it may be trivial to replace the coarse-grained technology in each of Wong's DPUs with an FPGA's fine-grained technology (*e.g.,* col. 5, lines 30-42), it is impossible to replace Wong's DPUs with respective FPGA chips. And an argument by the Examiner that it would be obvious to scale Wong's single-chip architecture to a multi-chip architecture so that one can replace the DPUs with FPGA chips would fail, because such scaling is not trivial, and Wong fails to teach or suggest how to perform such scaling or provide a reasonable expectation that such scaling would be successful.

Claims 8 and 14

These claims are patentable by virtue of their respective dependencies from claims 1 and 11.

Claim 23

New claim 23 recites a processor operable to retrieve program instructions via a program-instruction bus, and a pipeline accelerator inoperable to communicate directly with the program-instruction bus.

Neither Wong nor any other art of which the Applicants' attorney is aware teaches or suggests this limitation.

Claim 24

New claim 24 is patentable for reasons similar to those recited above in support of the patentability of claim 23.

Claims 25-27

These claims are patentable by virtue of their dependencies from claim 24.

CONCLUSION

In light of the foregoing, claims 2-3, 5-10, and 12-14 as previously pending, claims 1, 4, 11, and 15-22 as amended, and new claims 23-27 are in condition for full allowance, and that action is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

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Respectfully submitted,
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